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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,461	07/21/2003	Cherng-Chiao Wu	2410-0173P	5230

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EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/622,461	WU, CHERNG-CHIAO	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-7 and 10-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-7 and 10-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed on December 27, 2004.

Claim Objections

Claims 5 is objected to because of the following informalities: the last line of the claim contains the limitation "the other surface." There is insufficient antecedent basis for the limitations in the claims. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-6, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chun (US 6,407,448 B2) in view of Farnworth et al. (US 6,020,629).

In re claim 1, Chun shows (fig. 3-5A) a structure for stacking chip scale packages comprising a stack frame (25), the stack frame, a first chip scale package (1) being in the opening of the stack frame, the first chip scale package having legs (4c) soldered on the solder spots (at the end of 4c) of the stack frame, the first chip scale package and the stack frame being a first unit (100 in fig. 5A), at least a second unit (110) being stackable and soldered over the first unit, with a bottom of the first unit being soldered to a surface of a printed circuit board (col. 3, lines 52-58). Chun shows all of the elements

of the claims except the opening in the center of the substrate being a through hole. Farnworth et al. shows (figs. 1-2D) a semiconductor stacking apparatus having a substrate (22) with an opening being a through hole formed through the upper and lower surface of the substrate. With this configuration a semiconductor integrated circuit assembly can be formed in the substrate and configure to provided a planar surface to further facilitate stacking of the substrates (col. 2, lines 10-25). Farnworth also shows that the periphery of the cavity has solder spots (42RF) that are electrically connected to the other surface of the substrate through via (44) and connected to the printed circuit board through balls (42). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the substrate of Chun by forming the opening as a through hole as taught by Farnworth to form a planar IC assembly that would better facilitate stacking of subsequent stacking apparatuses.

In re claims 4-6, Farnworth shows (fig. 1-2D) that the periphery of the cavity has solder spots (38) that are electrically connected to the lower surface of the substrate through via (44) and connected to the printed circuit board through balls (42).

In re claims 11 and 12, Farnworth shows (figs. 1-2D) that the first unit and the second unit are soldered through the legs (40) of the first chip scale package of the first unit and legs of a second chip scale package of the second unit, the stack frame of the first unit having a bottom side bonding to a printed circuit board through solder balls (12). The legs of the first unit is soldered on the printed circuit board and the second unit has a second chip scale package, the second chip scale package having legs bonded to the solder spots on an upper surface of the stack frame of the first unit.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chun (US 6,407,448 B2) in view of Farnworth et al. (US 6,020,629) as applied to claim 1 above, and further in view of Brandenburg et al. (US 2004/0113281 A1).

In re claim 7, Chun in view of Farnworth shows all of the elements of the claims except the air vents communicating with the opening in the center. Brandenburg et al. discloses [0022] that air vents in a package allows unwanted air to escape the package during a subsequent molding process. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the substrate of Chun and Farnworth by forming air vents in the substrate as taught by Brandenburg to allow unwanted air or gas to escape the assembly during the molding or packaging process.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chun (US 6,407,448 B2) in view of Farnworth et al. (US 6,020,629) as applied to claim 1 above, and further in view of Harada et al. (US 2001/0054481 A1).

In re claim 10, Chun in view of Farnworth shows all of the elements of the claims except the bottom of a lower unit sinking into a cavity of the surface of the printed circuit board. Harada et al. discloses [0006-0007] that a cavity may be formed in a circuit board and have devices mounted therein to reduce the thickness of a multi-layered circuit board and ultimately reduce the size of an electronic device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the printed circuit board of Chun and Farnworth by forming a cavity within it as

taught by Harada to form assemblies within the cavity and ultimately reduce the size of the electronic device.

Claims are rejected under 35 U.S.C. 103(a) as being unpatentable over Chun (US 6,407,448 B2) in view of Park et al. (US 6,380,615 B1).

In re claim 13, Chun shows (fig. 3-5A) a structure for stacking chip scale packages comprising: a stack frame (25), the stack frame having an opening in the center of a upper surface of the stack frame and a plurality of solder spots (near 4c) located on the periphery of the opening, the solder spots being electrically connected to lower surface (27) of the stack frame; a first chip scale package (1), the first chip scale package being in the opening, the first chip scale package having legs (4c) soldered on the solder spots of the stack frame; and a second chip scale package (110). Chun shows all of the elements of the claims except the second chip scale package being contacting the first chip scale package. Park et al. shows (fig. 12) a chip stack package comprising a first chip scale package (20) in the recess of a stack frame (50) and a second chip scale package (20 on the top) contacting the first chip scale package. With this configuration the signal connection process is made simple (col. 2, lines 40-45) and the thickness of the package is reduced (col. 6, lines 48-51). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the stacking chip scale package of Chun by forming the second chip scale package contacting the first chip scale package within the stack frame as taught by Park to simplify the manufacturing process and reduce the overall device thickness.

In re claims 15, 17, and 18, Chun shows (fig. 3-5A) that the opening in the center of the stack frame is a cavity sunk from a surface of the stack frame, that the periphery of the cavity has solder spots (4c) that are electrically connected to the other surface of the stack frame, and that solder spots on the periphery of the cavity are electrically connected to a surface of the printed circuit board through solder balls (8b). In re claims 21, 22, and 23, with respect to the limitations concerning a second unit and a third chip scale package, It would have been obvious to one of ordinary skill in the art to use three, four, etc., stack units or chip scale packages since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).* See also MPEP 2144.04 VI. (B). Chun shows (fig. 3 and 4) that there are additional units (110, 120, etc) that stack onto the first unit and that the first unit as a bottom side for bonding to a printed circuit board (col. 3, lines 52-58).

Claims 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chun (US 6,407,448 B2) in view of Park et al. (US 6,380,615 B1) as applied to claim 13 above, and further in view of Farnworth et al. (US 6,020,629).

In re claims 14 and 15, Chun and Park show all of the elements of the claims except the opening in the center of the substrate being a through hole. Farnworth et al. shows (figs. 1-2D) a semiconductor stacking apparatus having a substrate (22) with an opening being a through hole formed through the upper and lower surface of the substrate. With this configuration a semiconductor integrated circuit assembly can be

formed in the substrate and configure to provided a planar surface to further facilitate stacking of the substrates (col. 2, lines 10-25). Farnworth also shows that the periphery of the cavity has solder spots (42RF) that are electrically connected to the other surface of the substrate through via (44) and connected to the printed circuit board through balls (42). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the substrate of Chun and Park by forming the opening as a through hole as taught by Farnworth to form a planar IC assembly that would better facilitate stacking of subsequent stacking apparatuses.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chun (US 6,407,448 B2) in view of Park et al. (US 6,380,615 B1) as applied to claim 13 above, and further in view of Brandenburg et al. (US 2004/0113281 A1).

In re claim 19, Chun and Park show all of the elements of the claims except the air vents communicating with the opening in the center. Brandenburg et al. discloses [0022] that air vents in a package allows unwanted air to escape the package during a subsequent molding process. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the substrate of Chun and Park by forming air vents in the substrate as taught by Brandenburg to allow unwanted air or gas to escape the assembly during the molding or packaging process.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chun (US 6,407,448 B2) in view of Park et al. (US 6,380,615 B1) as applied to claim 13 above, and further in view of Harada et al. (US 2001/0054481 A1).

In re claim 20, Chun and Park show all of the elements of the claims except the bottom of a lower unit sinking into a cavity of the surface of the printed circuit board. Harada et al. discloses [0006-0007] that a cavity may be formed in a circuit board and have devices mounted therein to reduce the thickness of a multi-layered circuit board and ultimately reduce the size of an electronic device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the printed circuit board of Chun and Park by forming a cavity within it as taught by Harada to form assemblies within the cavity and ultimately reduce the size of the electronic device.

Response to Arguments

Applicant's arguments filed with respect to the rejection of claims 2 and 4 over Chun and Farnworth (and now applied to claim 1) have been fully considered but they are not persuasive. The applicant asserts that Farnworth cannot be combined with Chun because Farnworth would destroy the function of Chun. The examiner believes that the combination is proper and all of the elements of the claims have been shown. Chun showed all of the elements of the claims except the through hole in the stack frame. As stated above, Farnworth disclosed a stack frame having a through hole to minimize the thickness of the package. Although Chun forms the solder ball connections

on the bottom of the stack frame, when combined with Farnworth those solder balls would be moved to the edges of the stack frame and out of the way of the chip scale package just as Farnworth shows in figures 2A-2C. Such a combination would not destroy the function of Chun but improve Chun because the stack frame and package would have a slimmer profile. The cited art shows all of the elements of the claims and this action is made final.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571)

272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
March 10, 2005

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER